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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,402	01/11/2002	Olivier Menut	00-GR1-239	8917

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FLEIT, KAIN, GIBBONS,
GUTMAN & BONGINI, P.L.
ONE BOCA COMMERCE CENTER
551 NORTHWEST 77TH STREET, SUITE 111
BOCA RATON, FL 33487

EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,402	MENUT ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species I, depicted in figures 1a – 1h and drawn to claims 1 – 10, 15 and 17, in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 10 recites the limitation "the silicon" in the second line of the claim. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action "the silicon" will be considered --sidewall surfaces of the trench--.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher et al. (USPAT 4942554, Kircher) in view of Jang et al. (USPAT 5637529, Jang).

With regard to claim 1, Kircher discloses a process for fabricating a semiconductor substrate with a single crystal lattice. Kircher discloses in figures 1 – 5 forming a substrate (1) with a single crystal lattice, the substrate having a top surface with at least one discontinuity in the single crystal lattice therein, whereby the top surface of the substrate has a recess (2) at the discontinuity on the top surface. Kircher discloses in figures 1 – 5 depositing a layer of amorphous material (8) having the same chemical composition as that of the substrate. Kircher discloses in figures 1 – 5 and column 4, lines 13 – 20 thermally annealing the amorphous material so as to be continuous with the single crystal lattice of the substrate. Kircher does not teach amorphizing the single crystal lattice around a periphery of the recess. Jang teaches in figure 1b amorphizing a single crystal lattice (31) around a periphery of a recess (39). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the amorphizing of Jang in the method of Kircher in order to remove lattice defects, thereby improving yield and productivity of the semiconductor device as stated by Jang in column 1, lines 45 – 50.

With regard to claim 2, Kircher discloses in column 4, lines 6 and 7 planarizing the top surface of the substrate.

With regard to claim 4, Kircher discloses in column 3, line 44 wherein the step of forming the substrate includes forming the substrate with at least part of the material of silicon.

With regard to claim 17, Kircher and Jang disclose an integrated circuit comprising a silicon substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface and whereby the surface is treated in accordance with the process of claim 1.

6. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher and Jang as applied to claims 1 and 2 above, and further in view of one of ordinary skill in the art.

With regard to 3, Kircher teaches a step of planarizing in column 4, lines 6 and 7. Kircher does not teach how the planarization is accomplished. It is well known in the art wherein a step of planarizing a top surface includes planarizing the top surface by a chemical mechanical polishing. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use chemical mechanical polishing in the method of Kircher and Jang in order to reliably produce a planar substrate thus improving device yields and device performance.

With regard to claim 5, Jang teaches in column 2, lines 50 – 60 wherein the step of amorphizing includes amorphizing with a localized ion implantation around the recess by a masking operation.

7. Claims 6 – 10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher and Jang as applied to claims 1 and 2 above, and further in view of Lill et al. (USPAT 6074954, Lill) and Numazawa et al. (USPAT 6168996, Numazawa).

With regard to claim 6, Kircher discloses in figures 1 – 5 wherein the step of forming a substrate include the sub-steps of etching a trench, and filling trench with a fill material so as to form the single-crystal lattice discontinuity. Kircher does not teach depositing first and second layers. Lill teaches in figures 3 – 13b depositing a first layer (6) of a first material and a second layer (8) of a second material in succession on a substrate (2), etching the first layer and an upper portion of a trench fill material (16) so as to form lateral cavities (22) in the second layer in communication with a trench (16) and so as to form the recess at a discontinuity (12). It would have been obvious to one of ordinary skill in the art to use the first and second layers of Lill in the method of Kircher and Jang in order to provide a mask for the etching of the trench as taught by Lill in column 10, line 56 – column 11, line 37. Kircher, Jang and Lill are silent to removing the second layer. Numazawa teaches in figures 21 and 22 removing a second layer (2b) it would have been obvious to one of ordinary skill in the art at the time of the present invention to use the removing of Numazawa in the method of Kircher, Jang and Lill in order to expose underlying layers for the production of devices that will communicate with the trench.

With regard to claim 7, Kircher discloses in figure 2 wherein the sub-step of filling of the trench with fill material includes filling the trench with at least part of the fill material of a silicon oxide (4).

With regard to claim 8, Kircher discloses in figure 2 wherein the sub-step of filling of the trench with fill material includes filling at least part of the trench with an insulating fill material.

With regard to claim 9, Lill teaches in figure 4, and column 11, liens 51 – 62 wherein a sub-step of filling the trench is carried out by depositing silicon oxide (10) as a conformal coating. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conformal coating of Lill in order to form a dielectric layer with a defect density low enough for improved performance of DRAM devices.

With regard to claim 10, Numazawa teaches in figure 19 wherein the sub-step of filling of the trench is carried out by thermal oxidation (5a) of the silicon. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thermal oxidation of Numazawa in order to use an efficient and inexpensive means at filling the trench that is proven to form a reliable film.

With regard to claim 15, Jang teaches in figure 1b wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1 – 3, 5 – 8, 10, 15, and 17 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, and 5 – 9 of U.S. Patent No. 6,537,873. Although the conflicting claims are not identical, they are not patentably distinct from each other because Claims 1 – 3, 5 – 8, 10, 15, and 17 is obvious over claim 1, and 5 – 9 of U.S. Patent No. 6,537,873 because all of the features of the pending claims are covered in the patented claims. The pending claims cover the subject matter of the patented claims, while the patented claims are more specific.

2. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,537,873 in view of Kircher. U.S. Patent No. 6,537,873 does not disclose that a material for the substrate. Kircher discloses in column 3, line 44 a silicon substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the silicon substrate in the method of Kircher in order to have a substrate material that is well understood and widely available in the art, thus saving money in research and development costs.

3. Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 5 and 6 of U.S. Patent No. 6,537,873 in view of Lill et al. (USPAT 6074954, Lill). U.S. Patent No. 6,537,873 discloses wherein the sub-step of filling the trench is carried out by thermal oxidation of the trench surface. U.S. Patent No. 6,537,873 does not disclose that the filling the trench if carried out by depositing silicon oxide as a conformal coating. Lill teaches in figure 4, and column 11, liens 51 – 62 wherein a sub-step of filling the trench is carried out by depositing silicon oxide (10)as a conformal coating. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conformal coating of Lill in the method of U.S. Patent No. 6,537,873 in order to form a dielectric layer with a defect density low enough for improved performance of DRAM devices.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chen et al., and Wanlass teach recrystallizing amorphous layers. Tarui et al. teach further amorphizing by ion implantation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
June 18, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800